AMENDMENTS TO THE CLAIMS

1-2. (Canceled)

3. (Currently amended) A method of operating a plurality of pixels of an image sensor comprising:

accumulating a first charge in a first photosensor;

transferring said first charge from said first photosensor to a first storage device;

transferring said first charge from said first storage device to a floating diffusion node;

reading out the first charge from said floating diffusion node;

accumulating a second charge in a second photosensor;

transferring said second charge from said second photosensor to a second storage device;

transferring said second charge from said second storage device to said floating diffusion node; and

reading out the second charge from said floating diffusion node,

wherein each of the first and second storage devices comprises a storage node and a capacitor, and

wherein transferring said respective charges from said respective photosensors to said respective storage devices comprises turning on a respective shutter transistor, a gate of which is connected to said capacitor and a drain of which is connected to said storage node of said respective storage device.

4. (Currently amended) The method of claim 3, wherein ~~a portion~~ said capacitor of said first and second storage devices reside above a substrate in which the first and second photosensors reside.

5. (Withdrawn) The method of claim 3 further comprising the act of sharing said floating diffusion node with a third and fourth pixel, wherein said floating diffusion node is reset, said third

pixel accumulates a third charge in a third photosensor, transfers said third charge from said third photosensor to a third storage device, transfers said third charge from said third storage device to said floating diffusion node and reads out the third charge from said floating diffusion node; and

wherein said floating diffusion node is reset, said fourth pixel accumulates a fourth charge in a fourth photosensor, transfers said fourth charge from said fourth photosensor to a fourth storage device, transfers said fourth charge from said fourth storage device to said floating diffusion node and reads out the fourth charge from said floating diffusion node.

6. (Original) The method of claim 3, wherein a readout circuit outputs the first and second charges by:

turning on a first transfer gate of a first pixel to transfer the first charge to the floating diffusion node, and turning on a row select transistor; and

turning on a second transfer gate of a second pixel after the readout of said first pixel to transfer the second charge to said floating diffusion node, and turning on said row select transistor.

7. (Withdrawn) The method of claim 6, wherein said transferring steps occur on half clock cycles.

8-18. (Canceled)

19. (Currently amended) A pixel circuit for use in an imaging device, said pixel circuit comprising:

a plurality of photosensors for generating charge during an integration period;

a plurality of shutter transistors, each shutter transistor connected to and transferring charge from a respective photosensor;

a plurality of storage nodes, wherein each storage node comprises a capacitor which is coupled to a respective shutter transistor via a shutter line and wherein each node stores[[ing]] charge transferred by a respective one of said plurality of photosensors;

a plurality of transfer transistors ~~gates~~, each transfer transistor ~~gate~~ connected to and transferring charge from a respective storage node;

a floating diffusion node connected to said plurality of transfer transistors ~~gates~~ for receiving charge from said transfer transistors ~~gates~~; and

a readout circuit connected to said floating diffusion node to output charge accumulated at the floating diffusion node.

20. (Currently amended) The circuit of claim 19 wherein said readout circuit further comprises a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node prior to receiving charge from a respective one said plurality of transfer transistors ~~gates~~.

21. (Currently amended) The circuit of claim 19, wherein said ~~storage nodes comprise~~ capacitors are formed above a substrate in which the floating diffusion node is formed.

22. (Original) The circuit of claim 21, wherein said capacitors are polypropylene capacitors.

23. (Original) The circuit of claim 19, wherein said shutter transistors operate as electronic shutters for said pixel.

24. (Original) The circuit of claim 19, wherein said shutter transistors remain on during the integration period.

25. (Original) The circuit of claim 19, wherein said pixel is a CMOS pixel.

26. (Original) The circuit of claim 19, wherein said pixel is a five transistor pixel.

27. (Currently amended) A pixel circuit for use in an imaging device, said pixel circuit comprising:

a photosensor for generating charge during an integration period;

a shutter transistor connected to said photosensor to transfer charge from said photosensor;

a storage node connected to said shutter transistor;

a storage capacitor connected [[to]] between a gate of said shutter transistor and said storage node, the storage capacitor [[to]] receiving[[e]] said charge transferred by said shutter transistor;

a transfer transistor ~~gate~~ connected to said storage node ~~capacitor~~ to transfer charge from said storage node ~~capacitor~~;

a floating diffusion node connected to said transfer transistor ~~gate~~ to receive said charge from said transfer transistor ~~gate~~;

a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node;

a source-follower transistor connected to said reset transistor for receiving charge from the floating diffusion node; and

a row select transistor connected to said source-follower transistor for outputting a signal produced by said source follower transistor.

28. (Currently amended) The circuit of claim 27, wherein a plurality of said photosensors, shutter transistors, storage capacitors and transfer transistors ~~gates~~ share said floating diffusion node, reset transistor, source follower transistor, and row select transistor.

29. (Original) The circuit of claim 27, wherein said pixel is a CMOS pixel.

30-41. (Canceled)

42. (Currently amended) An imaging system comprising:

a processor; and

an imaging device comprising an array of pixels, coupled to said imaging system comprising:

a plurality of photosensors for generating charge during an integration period;

a plurality of shutter transistors, each shutter transistor connected to and transferring charge from a respective photosensor;

a plurality of storage nodes, each storage node connected to a respective shutter transistor;

a plurality of storage capacitors, each capacitor coupled [[to]] between a gate of a respective shutter transistor and a respective storage node, the storage capacitor [[and]] storing charge transferred by a respective one of said plurality of photosensors;

a plurality of transfer transistors ~~gates~~, each transfer transistor ~~gate~~ connected to and transferring charge from a respective storage node ~~capacitor~~;

a floating diffusion node connected to said plurality of transfer transistors ~~gates~~ for receiving charge from said transfer transistors ~~gates~~; and

a readout circuit connected to said floating diffusion node to output charge accumulated at the floating diffusion node.

43. (Original) The system of claim 42, wherein a number of said plurality of photosensors is two photosensors.

44. (Withdrawn) The system of claim 42, wherein a number of said plurality of photosensors is four photosensors.

45. (Original) The system of claim 42, wherein said shutter transistor is an electronic shutter.

46. (Original) The system of claim 42, wherein said shutter transistor remains on during the integration period.

47. (Original) The system of claim 42, wherein said capacitors are polypropylene capacitors.

48. (Original) The system of claim 42, wherein said imaging system is a CMOS imaging system.

49. (New) The circuit of claim 19 wherein said capacitor of each storage node is coupled to a gate portion of said respective shutter transistor.